Patent claims

1. An arrangement applied to a node in a communication network, said node comprising one or more time-slot buses transferring frames from a number of serial input lines located on a receiving side of the node to a number of serial output lines located on the transmitting side of the node,
characterized in

one or two data buffers for each time-slot bus at the receiving side buffering the frames from the input lines before transmission,

connection table for each time-slot bus at the receiving side, each entry in the connection table containing at least a data address pointing to a byte in the associated data buffer, the entries are arranged in the same order as their corresponding bytes are to be transferred on the data bus, and

a counter, synchronized to a clock used by the time-slot bus for transmission of time slots, indicating which byte in the associated data buffer that presently is to be read out from the data-bus buffer into a time slot in the associated data bus by indexing the entries of the connection table.

2. Arrangement according to claim 1,
characterized in that the data buffers are shared between all the input lines by means of respective pointers allocating one memory area in the data buffer for each of the input lines.

3. Arrangement according to claim 1 or 2,
characterized in that each entry in the connection table contains, in addition to the data address, a control field.

4. Arrangement according to any of the preceding claims, c h a r a c t e r i z e d i n that there is only one data buffer for each time slot bus, and, within the same frame, a data location in the buffer is not read before write-in.

5. An arrangement applied to a node in a communication network, said node comprising one or more time slot buses transferring frames from a number of serial input lines located on a receiving side of the node to a number of serial output lines located on the transmitting side of the node,
c h a r a c t e r i z e d i n

one or two data buffers for each time-slot bus at the transmitting side buffering the frames from time-slot buses before forwarding to the output line,

a connection table wherein each entry in the connection table contains at least a data address pointing to a byte in one of the data buffers, the entries are arranged in the same order as their corresponding bytes are to be transferred to an output line.

6. Arrangement according to claim 5,
c h a r a c t e r i z e d i n

one starting pointer per output line allocating one memory area in the connection table for each of the output lines, and pointing to the first entry in each memory area,

one indexing pointer per output line pointing at the entry in the connection table holding the address to the byte currently being fetched from one of the buffers to the associated output line.

7. Arrangement according to claim 5 or 6, c h a r a c t e r i z e d i n that each entry in the connection table contains, in addition to the data address, a control field.

8. Arrangement according to one of the claims 5 - 7, c h a r a c t e r i z e d i n that there is only one data buffer for each time-slot bus, and, within the same frame, a data location in the buffer is not read before write-in.

9. Arrangement according to one of the claims 5 - 8, c h a r a c t e r i z e d i n that there is only one data buffer for each time-slot bus, and, within the same frame, a data location in the buffer is not read before write-in.